IN THE CLAIMS:

1. An integrated circuit comprising an on-chip decoupling capacitor located over a topmost metal interconnect level.

2. An integrated circuit, comprising:

at least one lower metal interconnect level located over a semiconductor body;

a topmost metal interconnect level located over said lower metal interconnect level, said topmost metal interconnect level comprising a first and a second metal interconnect line;

a bottom electrode located over and in electrical contact with said first metal interconnect line;

a capacitor dielectric located over said bottom electrode; and

a top electrode located over said capacitor dielectric.

3. The integrated circuit of claim 2, further comprising a metal cap layer located over said top electrode and said topmost metal interconnect level, said metal cap layer electrically connecting said top electrode and said second metal interconnect line.

4. The integrated circuit of claim 3, wherein said metal cap layer comprises aluminum.

5. The integrated circuit of claim 2, wherein said top electrode comprises TaN, said capacitor dielectric comprises tantalum-oxide, and said bottom electrode comprises TaN.

6. The integrated circuit of claim 2, wherein the top and bottom electrodes each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ir, Ru, and Ta.

7. The integrated circuit of claim 2, wherein the capacitor dielectric comprises hafnium-oxide.

8. The integrated circuit of claim 2, wherein the capacitor dielectric comprises silicon-nitride.

9. An integrated circuit comprising:

a plurality of lower copper interconnect levels located over a semiconductor body;

a topmost copper interconnect level located over said plurality of lower copper interconnect levels, said topmost copper interconnect level comprising a first and a second copper interconnect line;

a bottom electrode in direct contact with said first copper interconnect line;

a capacitor dielectric located over said bottom electrode;

a top electrode located over said capacitor dielectric;

a protective overcoat located over said topmost copper interconnect level; and

an aluminum cap layer located, in part, over said protective overcoat and electrically connecting said top electrode and said second copper interconnect line.

10. The integrated circuit of claim 9, wherein said top electrode comprises TaN, said capacitor dielectric comprises tantalum-oxide, and said bottom electrode comprises TaN.

11. A method of fabricating an integrated circuit comprising the steps of:

providing a semiconductor body having a plurality of metal interconnect levels formed thereon, a topmost one of said plurality of metal interconnect levels having a first and a second metal interconnect line; and

forming a decoupling capacitor over said topmost one of said plurality of metal interconnect levels.

12. The method of claim 11, wherein a bottom electrode of said decoupling capacitor is electrically connected to said first metal interconnect line.

13. The method of claim 11, further comprising the step of forming a metal capping layer over said topmost one of said plurality of metal interconnect levels and said decoupling capacitor, wherein said metal capping layer electrically connects a top electrode of said decoupling capacitor to said second metal interconnect line.

14. The method of claim 11, wherein said step of forming said decoupling capacitor comprises the steps of:

forming a bottom electrode material over said topmost one of said plurality of metal interconnect levels;

forming a capacitor dielectric over said bottom electrode material; and

forming a top electrode material over said capacitor dielectric.

15. The method of claim 14, wherein said top electrode comprises TaN, said capacitor dielectric comprises tantalum-oxide, and said bottom electrode comprises TaN.

16. The method of claim 14, wherein said step of forming a capacitor dielectric comprises the steps of:

depositing a layer of tantalum-oxide over said bottom electrode; and

annealing said layer of tantalum-oxide in oxygen to reduce impurities and increase the oxygen content.

17. A method of fabricating an integrated circuit comprising the steps of:

providing a semiconductor body having a plurality of copper interconnect levels formed therein, a topmost one of said plurality of copper interconnect levels having a first and a second copper interconnect line;

forming a bottom electrode material over said topmost one of said plurality of copper interconnect levels, said bottom electrode in direct contact with said first copper interconnect level;

forming a capacitor dielectric over said bottom electrode material;

forming a top electrode material over said capacitor dielectric;

patterning and etching the capacitor stack

forming an aluminum cap layer over said topmost one of said plurality of copper interconnect levels and said top electrode, wherein said aluminum cap layer electrically connects said top electrode to said second copper interconnect line.

18. The method of claim 17, wherein said top electrode comprises TaN, said capacitor dielectric comprises tantalum-oxide, and said bottom electrode comprises TaN.

19. The method of claim 17, wherein said step of forming a capacitor dielectric comprises the steps of:

depositing a layer of tantalum-oxide over said bottom electrode; and

annealing said layer of tantalum-oxide in oxygen.

20. The method of claim 17, wherein said top and bottom electrodes each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ir, Ru, and Ta.